SDLS076

SN54195, SN54LS195A, SN54S195, SN74195, SN74LS195A, SN74S195 4-BIT PARALLEL-ACCESS SHIFT REGISTERS

MARCH 1974-REVISED MARCH 1988

· Synchronous Parallel Load

- Positive-Edge-Triggered Clocking
- Parallel Inputs and Outputs from Each Flip-Flop
- Direct Overriding Clear
- . J and K Inputs to First Stage
- Complementary Outputs from Last Stage
- For Use in High Performance:
 Accumulators/Processors
 Serial-to-Parallel, Parallel-to-Serial
 Converters

description

These 4-bit registers feature parallel inputs, parallel outputs, $J \cdot \overline{K}$ serial inputs, shift/load (SH/ \overline{LD}) control input, and a direct overriding clear. All inputs are buffered to lower the input drive requirements. The register has two modes of operation:

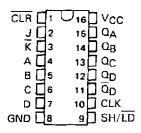
Parallel (broadside) load Shift (in the direction Q_A toward Q_D)

Parallel loading is accomplished by applying the four bits of data and taking SH/\overline{LD} low. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

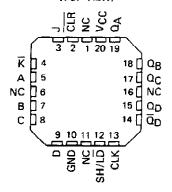
Shifting is accomplished synchronously when SH/ $\overline{\text{LD}}$ is high. Serial data for this mode is entered at the J- $\overline{\text{K}}$ inputs. These inputs permit the first stage to perform as a J- $\overline{\text{K}}$, D-, or T-type flip-flop as shown in the function table.

The high-performance '\$195, with a 105-megahertz typical maximum shift-frequency, is particularly attractive for very-high-speed data processing systems. In most cases existing systems can be upgraded merely by using this Schottky-clamped shift register.

SN54195, SN54LS195A, SN54S195...J OR W PACKAGE SN74195...N PACKAGE SN74LS195A, SN74S195...D OR N PACKAGE (TOP VIEW)



SN54LS195, SN54S195...FK PACKAGE (TOP VIEW)



NC - No internal connection

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
195	39 MHz	195 mW
'LS195A	39 MHz	70 mW
'\$195	105 MHz	350 mW

FUNCTION TABLE

		INP	UTS							0	UTPU	TS	
CLEAR	SHIFT/	01.001	SEF	IIAL	P.	AR/	ALL I	EL					<u> </u>
CLEAR	LOAD	CLOCK	J	ĸ	Α	В	C	D	QA	Q _B	QC	σo	ΩD
L	х	×	х	×	×	×	Х	Х	L	L	L	L	Н
н	L	t	х	x	а	ь	C	đ	а	b	c	d	ď
н	н	L	Х	х	х	Х	х	Х	QAO	G B0	α_{C0}	α_{D0}	$\bar{\alpha}_{D0}$
н	н	Ť	L	н	×	Х	Х	×	QAD	α_{A0}	σ_{Bn}	α_{Cn}	$\overline{\Omega}_{Cn}$
н	H	1	L	L	X	Х	Х	X	L	\mathbf{Q}_{An}	\mathbf{q}_{Bn}	α_{Cn}	$\bar{\alpha}_{Cn}$
н	н	1	н	н	х	х	Х	Х	н	α_{An}	QBn	α_{Cn}	$\bar{\alpha}_{Cn}$
н]	н	1	H	L	x	X	х	х	ā _{An}		α_{Bn}		\overline{a}_{Cn}

H = high level (steady state)

L = low level (steady state)

X = irrelevant (any input, including transitions)

† = transition from low to high level

a, b, c, d = the level of steady-state input at A, 8, C, or D, respectively

 $Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0}$ = the level of Q_{A}, Q_{B}, Q_{C} or Q_{D} , respectively, before the indicated steady state input conditions

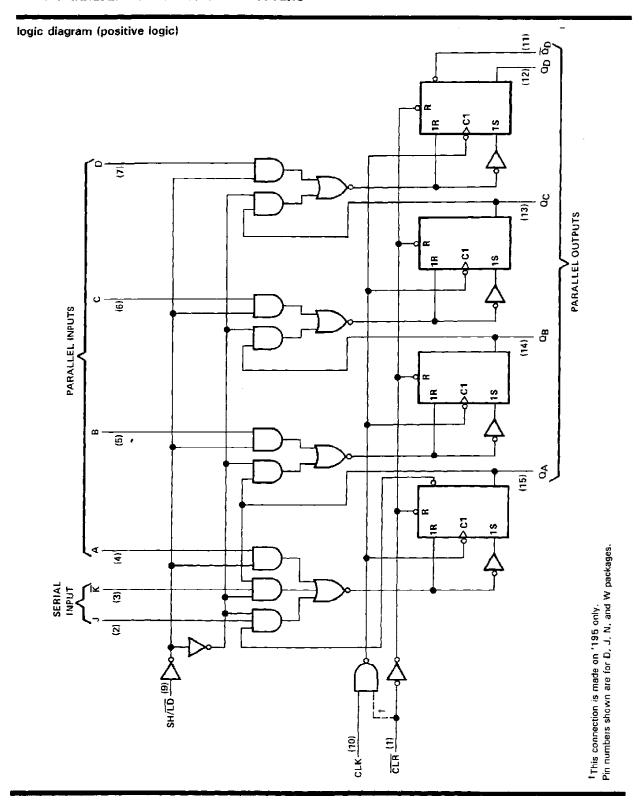
were established

or QCn = the level of QA. Qn. or (

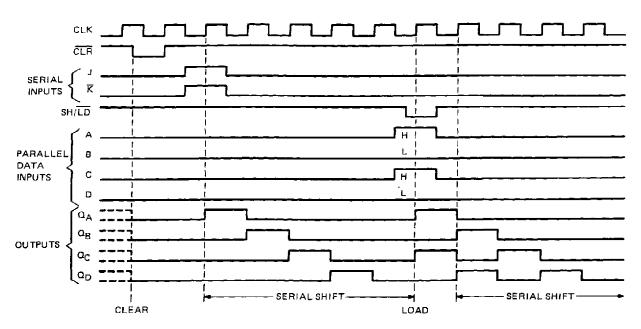
 q_{An}, q_{Bn}, q_{Cn} = the level of q_{A}, q_{B} , or q_{C} , respectively, before the most-recent transition of the clock

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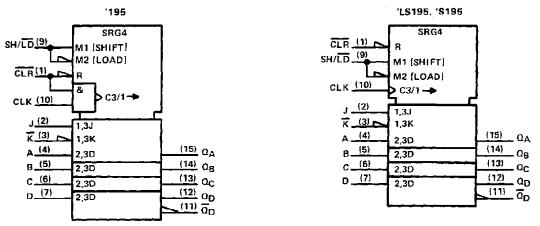




typical clear, shift, and load sequences



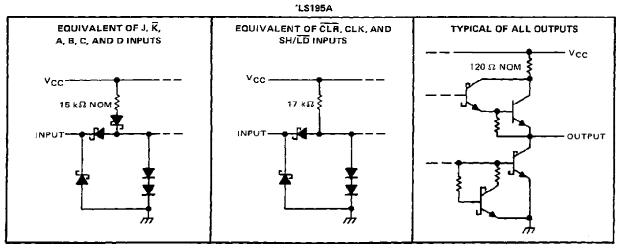
logic symbols†

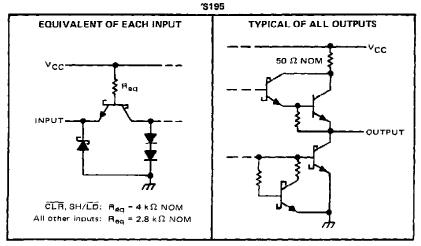


 7 These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12. Pin numbers are for D, J, N, and W packages.

SN54195, SN54LS195A, SN54S195, SN74195, SN74LS195A, SN74S195 4-BIT PARALLEL-ACCESS SHIFT REGISTERS

Schematics of inputs and outputs EQUIVALENT OF EACH INPUT TYPICAL OF ALL OUTPUTS VCC 100 Ω NOM Clock input: Req = 4 kΩ NOM All other inputs: Req = 6 kΩ NOM





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1)			 			 :							7 V
Input voltage	<i>.</i>	. ,							-			. 5	.5 V
Operating free-air temperature range:	SN54195		 								-55°C	to 12	2 5° C
	SN74195			÷							. 0°C	to 7	70°C
Storage temperature range											-65°C	to 15	in°c

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	· · · · · · · · · · · · · · · · · · ·		SN5419	5		SN7419	15	
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Supply voltage, VCC		4.5	5	5.5	4.75	5	5.25	٧
High-level output current, IOH				-800			-800	μА
Low-level output current, IOL				16	<u> </u>		16	mA
Clock frequency, f _{clock}		0		30	0		30	MHz
Width of clock input pulse, tw(clock)		16			16			пѕ
Width of clear input pulse, tw(clear)		12			12			ηs
	Shift/load	25			25			
Setup time, t _{su} (see Figure 1)	Serial and parallel data	20			20			ns
	Clear inactive-state	25			25			
Shift/load release time, t _{release} (see Figure 1)				10			10	n\$
Serial and parallel data hold time, th (see Figure 1)		0			0			ns
Operating free-air temperature, TA		-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
ViH	High-level input voltage		2			V
VIL	Low-level input voltage			•	0.8	V
VIK	Input clamp voltage	V _{CC} = MIN, I _I = -12 m	Δ		-1.5	V
VOH	High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -80	2.4	3.4		V
VOL	Low-level output voltage	$V_{CC} = MIN$, $V_{IH} = 2 V$, $V_{IL} = 0.8 V$, $I_{OL} = 16 m$	A	0.2	0.4	V
T ₁	Input current at maximum input voltage	V _{CC} = MAX, V ₁ = 5.5 V			1	mA
'ин	High-level input current	V _{CC} = MAX, V ₁ = 2.4 V			40	μА
l _{IL}	Low-level input current	V _{CC} = MAX, V _I = 0.4 V			-1.6	mA
loc	Short-circuit output current §	SNS	4195 -20		-57	_
los —	Office Contact Contact	VCC = MAX SN2	4195 - 18		-57	mA
Icc	Supply current	VCC = MAX, See Note 2		39	63	mA

 $^{^\}dagger$ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions,

switching characteristics, VCC = 5 V, TA = 25°C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
fmax	Maximum clock frequency	C ₁ = 15 pF,	30	39		MHz
[‡] PHL	Propagation delay time, high-to-low-level output from clear	1 _ - i		19	30	Π5
^t PLH	Propagation delay time, low-to-high-level output from clock	$R_{\perp} = 400 \Omega$, See Figure 1		14	22	ns
tPHL	Propagation delay time, high-to-low-level output from clock	See Figure 1		17	26	ns



[‡]All typical values are at V_{CC} = 5 V, T_A = 25°C.

[§]Not more than one output should be shorted at a time.

NOTE 2: With all outputs open, shift/load grounded, and 4.5 V applied to the J. K, and data inputs. I_{CC} is measured by applying a momentary ground, followed by 4.5 V, to clear and then applying a momentary ground, followed by 4.5 V, to clock.

SN54LS195A, SN74LS195A 4-BIT PARALLEL-ACCESS SHIFT REGISTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1)									7 V
Input voltage									
Operating free-air temperature range:	SN54LS195A								-55°C to 125°C
	SN74LS195A								. 0°C to 70°C
Storage temperature range				 					-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SI	154LS1	95A	AS .	174LS1	95A	UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	UNII
Supply voltage, VCC		4.5	5	5.5	4.75	5	5.25	V
High-level output current, IOH				-400			-400	μА
Low-level output current, IOL		1		4			8	mA
Clock frequency, fclock		0		30	0		30	MHz
Width of clock or clear pulse, tw(clock)		16			16			ns
Width of clear input pulse, tw(clear)		12			12			ns
	Shift/load	25			25			
Setup time, t _{SU} (see Figure 1)	Serial and parallel data	15			15			ns
	Clear inactive-state	25			25			
Shift/load release time, trelease (see Figure 1)				10			20	n\$
Serial and parallel data hold time, th (see Figure 1)		0			0			ns
Operating free-air temperature, TA		-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	De DetecTCD	7	ST CONDITIO	auct	SN	54LS19	5A	SN	74LS19	5A	
	PARAMETER	16.	21 COMPITIE	. 6 817	MIN	TYP [‡]	MAX	MIN	TYP‡	MAX	UNIT
VIH	High-level input voltage	1		• •	2		_	2			V
VIL	Low-level input voltage						0.7			0.8	V
Vik	Input clamp voltage	V _{CC} = MIN,	lj ≈ –18 mA				-1.5	l		⊸1.5	V
Vон	High-level output voltage	V _{CC} = MIN, V _{IL} = V _{IL} max,	V _{IH} = 2 V, I _{OH} = -400	μА	2.5	3.4		2.7	3.4		٧.
		VCC = MIN,	V _{IH} = 2 V,	I _{OL} = 4 mA		0.25	0.4		0.25	0.4	V
VOL	Low-level output voltage	VIL = VIL max		IOL = 8 mA					0.35	0.5	,
I _I	Input current at maximum input voltage	V _{CC} = MAX.	V1 = 7 V	•			0.1			0.1	πΑ
44	High-leval input current	VCC = MAX.	V ₁ = 2.7 V		7		20			20	μА
HL	Low-level input current	VCC - MAX,	V _I = 0.4 V				-0.4			-0.4	mА
los	Short-circuit output current §	V _{CC} = MAX			-20		-100	-20		-100	mA
Icc	Supply current	V _{CC} = MAX,	See Note 2			14	21		14	21	mΑ

¹ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics, VCC = 5 V, TA = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max} Maximum clack frequency	C ₁ = 15 pF,	30	39		MHz
tPHL Propagation delay time, high-to-low-level output from clear	$R_1 = 2 k\Omega$		19	30	ns
tpLH Propagation delay time, low-to-high-level output from clock	See Figure 1		14	22	ns
tPHL Propagation delay time, high-to-low-level output from clock	Gee (igure)		17	26	ns



^{*}All typical values are at V_{CC} = 5 V, T_A = 25 C.

Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second,

NOTE 2: With all outputs open, shift/load grounded, and 4.5 V applied to the J. K, and data inputs, I_{CC} is measured by applying a momentary ground, followed by 4.5 V, to clear and then applying a momentary ground, followed by 4.5 V, to clear and then applying a momentary ground.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1) .											7 V
Input voltage											
Operating free-air temperature range:	SN54S195						 				~55°C to 125°C
	SN74S195						. ,	-			. 0°C to 70°C
Storage temperature range							 		_		~65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		S	N54819	95	5	N74S1	95	
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Supply voltage, VCC		4.5	5	5.5	4.75	5	5.25	V
High-level output current, IOH				-1			-1	mΑ
Low-level output current, OL		1		20		·	20	mA
Clock frequency, f _{clock}		0		70	0		70	MHz
Width of clock input pulse, tw(clock)		7			7			ПŞ
Width of clear input pulse, tw(clear)		12			12			ns
	Shift/load	11			11			
Setup time, t _{su} (see Figure 1)	Serial and parallel data	5			5			ns
	Clear inactive-state	9			9			
Shift/load release time, trelease (see Figure 1)	_	1		2			6	ns
Serial and parallel data hold time, th (see Figure 1)		3			3			ns
Operating free-air temperature, TA		-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS [†]			MIN	TYP‡	MAX	UNIT
VIH	High-level input voltage				2			_v_
VIL	Low-level input voltage						0.8	V
ViK	Input clamp voltage	VCC = MIN,	I _I = -18 mA				-1.2	٧
Vон	High-level output voltage	V _{CC} = MIN,	V _{IH} = 2 V, I _{OH} = -1 mA	SN54S195	2.5	3.4		V
		V _{IL} = 0.8 V,		SN74S195	2.7	3.4		V
VOL	Low-level output voltage	V _{CC} = MIN,	V _{IH} = 2 V,				0.5	V
		VIL = 0.8 V,	1 _{OL} = 20 mA		ŀ			
1 ₁	Input current at maximum input voltage	V _{CC} - MAX,	V ₁ = 5.5 V				î	mA
ин	High-level input current	V _{CC} = MAX,	V _I = 2.7 V				50	μА
IL	Low-level input current	V _{CC} = MAX.	V _I = 0.5 V				-2	mΑ
los	Short-circuit output current §	V _{CC} = MAX			-40		-100	mA
lcc	Supply current	V _{CC} = MAX,	See Note 2	SN54S195		70	99	1
				SN74S195		70	109	mΑ

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics, VCC = 5 V, TA = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max} Maximum clock frequency	C ₁ = 15 pF,	70	105		MHz
tpht Propagation delay time, high-to-low-level output from clear			12.5	18.5	ns
tPLH Propagation delay time, low-to-high-level output from clock	See Figure 1		8	12	N5
tpHL Propagation delay time, high-to-low-level output from clock	Des l'igure i		11	16.5	D5

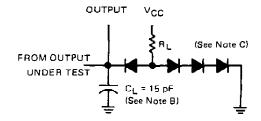


[‡]All typical values are at V_{CC} = 5 V, T_A = 25°C.

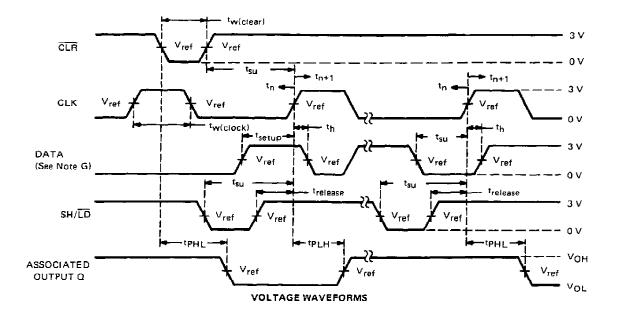
Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2: With all outputs open, shift/load grounded, and 4.5 V applied to the J. K, and data inputs, I_{CC} is measured by applying a momentary ground, followed by 4.5 V, to clear, and then applying a momentary ground, followed by 4.5 V, to clock.

PARAMETER MEASUREMENT INFORMATION



LOAD FOR OUTPUT UNDER TEST



NOTES: A. The clock pulse generator has the following characteristics: $Z_{\text{out}} \approx 50~\Omega$ and PRR \leq 1 MHz. For '195, $t_{\text{f}} \leqslant$ 7 ns and $t_{\text{f}} \leqslant$ 7 ns, For 'LS195A, $t_{\text{f}} \leqslant$ 15 ns and $t_{\text{f}} \leqslant$ 6 ns. For 'S195, $t_{\text{f}} \approx$ 2.5 ns and $t_{\text{f}} =$ 2.5 ns. When testing f_{max} , vary the clock PRR.

- B. C₁ includes probe and jig capacitance.
- C. All diodes are 1N3064 or equivalent.
- D. A clear pulse is applied prior to each test.
- E. For '195 and 'S195, $V_{ref} = 1.5 V$; for 'LS195A, $V_{ref} = 1.3 V$.

 F. Propagation delay times (tplH and tpHL) are measured at t_{n+1} . Proper shifting of data is verified at t_{n+4} with a functional test.
- G. J and K inputs are tested the same as data A, B, C, and D inputs except that shift/load input remains high.
- H. t_n = bit time before clocking transition.
 - t_{n+1} = bit time after one clocking transition.
 - t_{n+4} = bit time after four clocking transitions.

FIGURE 1-SWITCHING TIMES



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